RAITON

Silicon execution. Engineered to sign off.

Front-end design, verification, FPGA validation and embedded software services.

COMPANY PROFILE • BANGALORE, INDIA

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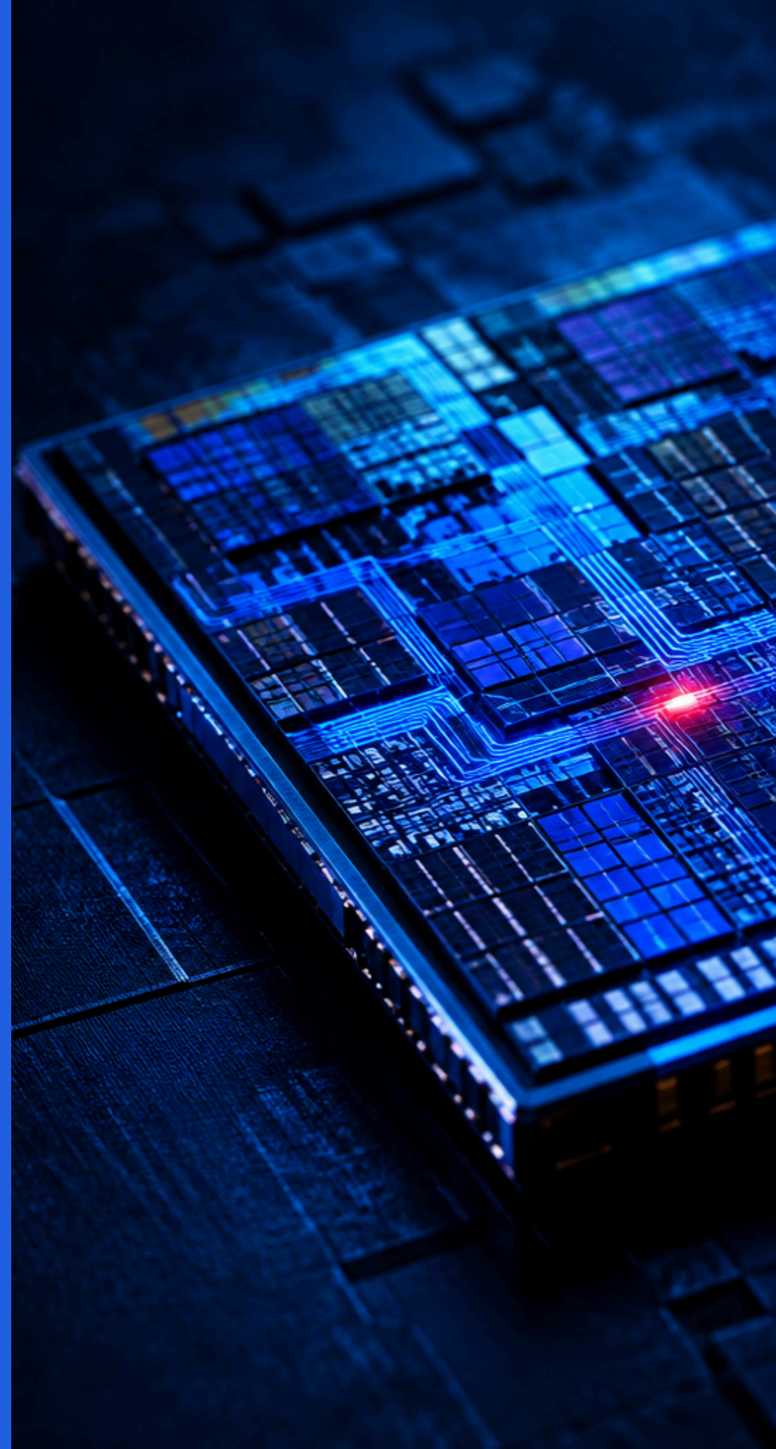
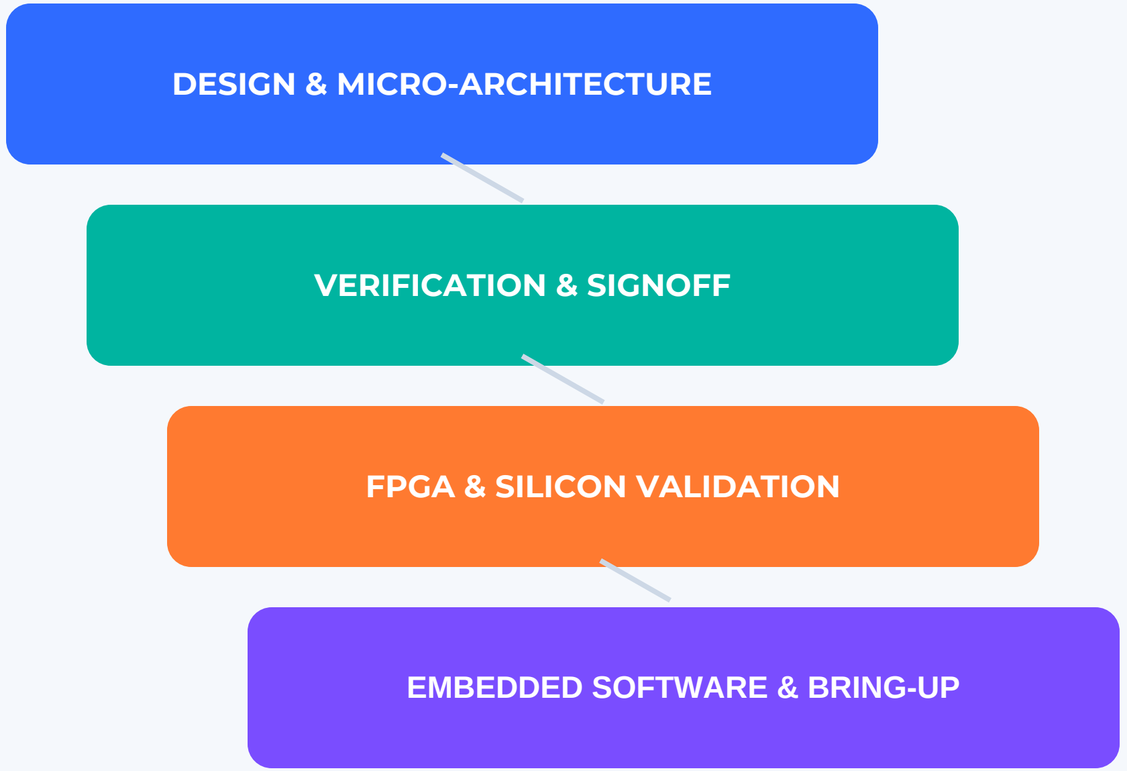


Your silicon execution partner

Bangalore-based. Built for AI-native semiconductor teams.

From specification to working silicon.

Raiton brings RTL design, verification, FPGA validation and embedded software expertise into one accountable execution layer — accelerating SoC programmes from spec to first boot without adding coordination drag.



Raiton at a glance

Focused capability. Senior execution. Built for complex silicon.

4

EXECUTION LAYERS

Design • DV • FPGA • Embedded

100+

ENGINEERS

Led by 13–18 yr practice heads

ASIL-D

SAFETY DEPTH

ISO 26262 aligned

Gen5

INTERFACE REACH

PCIe Gen3 / 4 / 5

Trusted on programmes at

Our engineers are embedded in demanding verification programmes across the semiconductor ecosystem.

- AI SILICON CO.
- AUTOMOTIVE SoC
- GLOBAL CPU IP
- EDGE COMPUTE
- NETWORKING ASIC
- MEMORY SYSTEMS
- MOBILITY CHIPSET
- INDUSTRIAL MCU

What we offer

One partner across the front-end silicon lifecycle — RTL to first boot.

DV SoC verification

UVM, formal, coverage closure

VL FPGA validation

Prototyping, emulation, post-silicon

RV Core verification

RISC-V and ARM cores

FS Functional safety

ASIL-D verification strategy

LP Low-power DV

UPF, XPROP, power intent

FW Embedded software

Bootloader, BSP, RTOS, drivers

Front-end services portfolio

Depth in every discipline between a specification and bootable silicon.

DESIGN & MICRO-ARCHITECTURE

RTL design & IP integration
Micro-architecture & specs
AXI • CHI • NoC interconnect
Low-power intent (UPF)
Lint • CDC • RDC clean
Synthesis-ready handoff

VERIFICATION & SIGNOFF

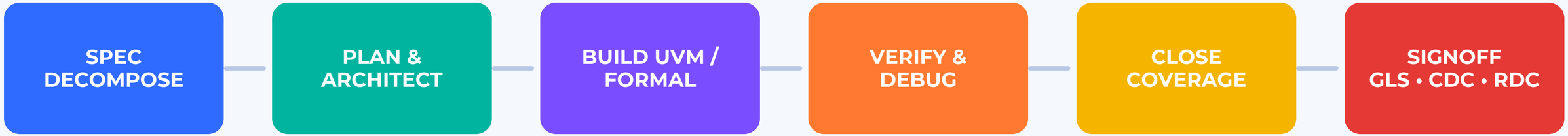
UVM testbench & VIP build
Formal property verification
Coverage-driven closure
Low-power & XPROP checks
Functional safety to ASIL-D
GLS & signoff evidence

VALIDATION & EMBEDDED

FPGA prototyping & emulation
SoC & board bring-up
Bootloader, BSP & RTOS / Linux
Drivers & protocol stacks
Post-silicon validation & debug
Firmware-assisted validation

Hardware verification services

Spec to signoff — a closed-loop execution model.



Verification IP • Assertions • Coverage • Regression • Debug • Signoff evidence

Pre & post silicon validation

Find issues earlier. Bring silicon up faster.

01 FPGA prototyping & emulation

02 Test-plan and diagnostics

03 Board bring-up & lab debug

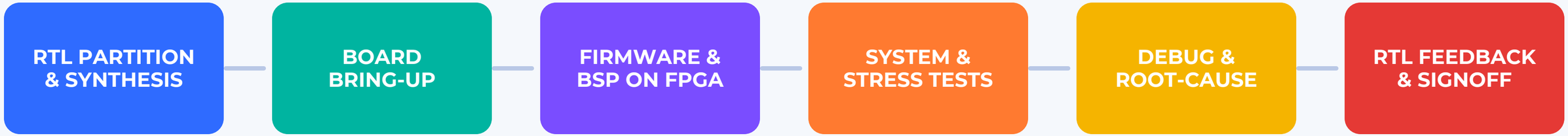
04 Performance and stress validation

05 Firmware-assisted validation



FPGA validation & emulation

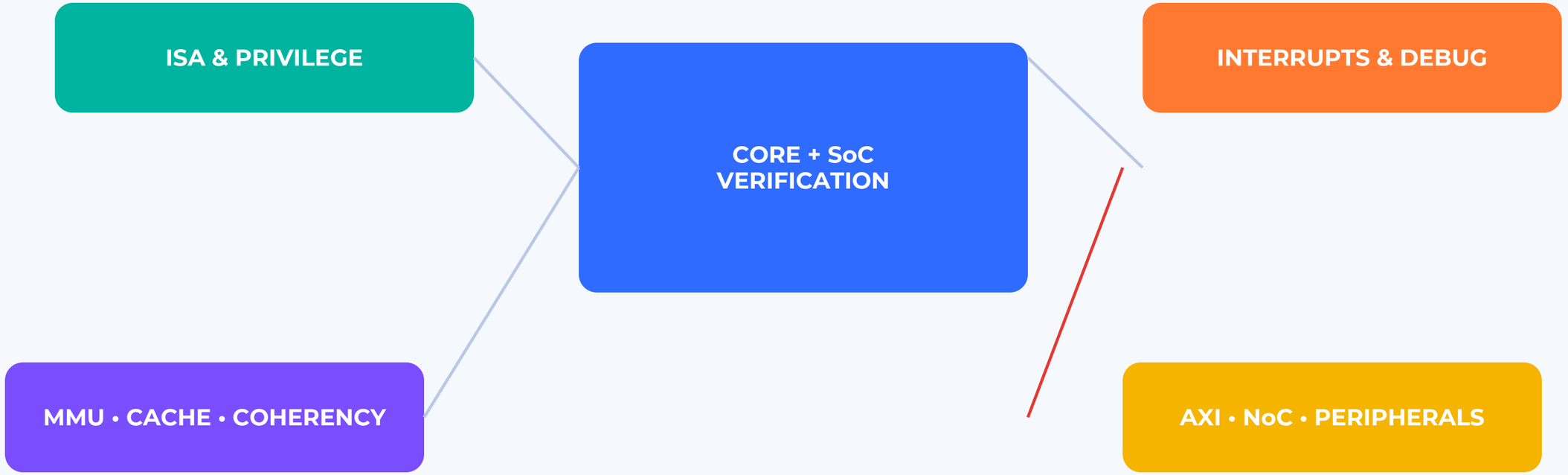
Run real software on the RTL months before tape-out — and feed every finding back to design.



AMD / Intel FPGA • VCS co-simulation • JTAG / Lauterbach • Logic analyser • CI/CD regression • 200+ configs

RISC-V core & SoC verification

Architecture-aware verification for modern compute subsystems.



Functional safety verification up to ASIL-D

Safety evidence engineered into verification — not added at the end.



Safety planning

ISO 26262 / IEC 61508 alignment

Fault campaigns

Injection, detection and diagnostic coverage

Safety mechanisms

Lockstep, ECC, watchdogs, redundancy

Evidence closure

Traceability, metrics and signoff artefacts

AI SoC execution areas we support

AI SoC AREA	RAITON EXPERIENCE
Core & Functional Safety	RISC-V / ARM Cortex-M/R • ASIL-D lockstep • ECC
High-Speed Interfaces	PCIe Gen3/4/5 • NVMe
Memory Subsystems	DDR4/5 • HBM
Data Movement	DMA engines • AXI • NoC
AI Accelerator Flows	ML SoC subsystem validation
Power Optimization	UPF • XPROP • low-power DV
FPGA & Emulation	Prototyping • VCS co-sim • GLS • CDC • RDC signoff
Embedded Software	Bootloader • BSP • RTOS / Linux • BLE / Wi-Fi stacks • Drivers

Case study: AI/ML SoC verification

Turning a complex accelerator subsystem into signoff-ready evidence.

CHALLENGE

Multi-engine AI subsystem with evolving specs, deep data paths and coverage risk.

RAITON EXECUTION

Built scalable UVM environments, assertion strategy and coverage-led regression closure.

CUSTOMER IMPACT

Faster debug cycles, clearer risk visibility and predictable verification signoff.

Case study: low-power ADAS SoC

Power intent, safety and silicon readiness — verified together.

SCOPE

Low-power automotive SoC with safety islands, power domains and mixed reset strategy.

EXECUTION

UPF checks, XPROP, isolation and retention verification, CDC/RDC and fault campaigns.

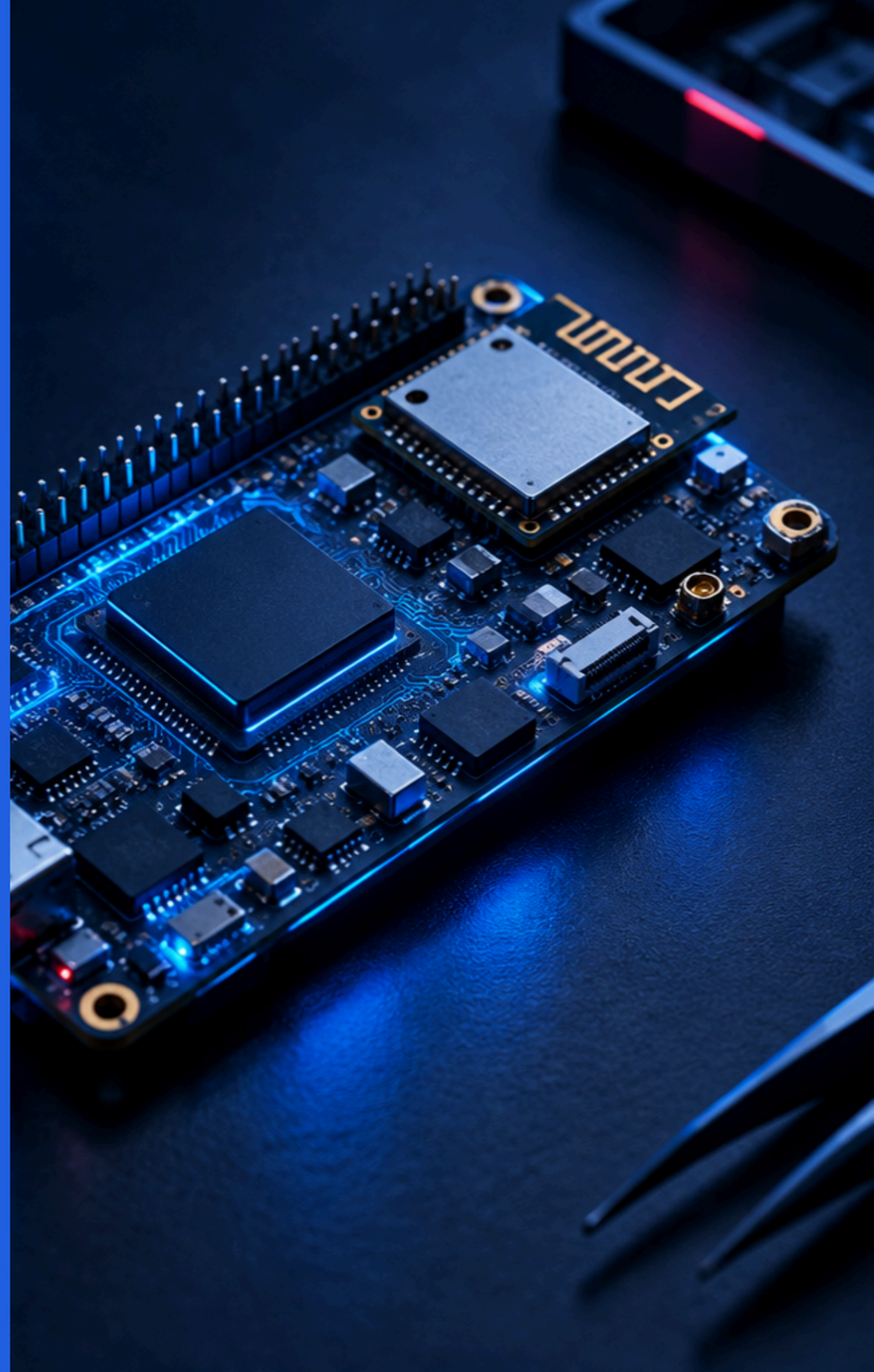
WHY IT MATTERS

Reduced escape risk where power transitions and safety mechanisms intersect.

Beyond verification: embedded software

Firmware and silicon aligned from day one — led by an 18-year embedded practice shipped on ARM and RISC-V SoCs.

Bootloader • BSP • RTOS / Linux (Yocto)
Drivers • BLE / Wi-Fi stacks • Embedded ML



Embedded practice at a glance

Senior firmware leadership with a track record from Tier-1 semiconductor and CPU-IP companies.

18+

YEARS EMBEDDED

Firmware, drivers, BSP, RTOS

200+

CORE-IP CONFIGS

BSP + validation, 1 to 16 cores

30

ENGINEERS LED

PMP & CMMI-audited delivery

BT 5

QUALIFIED STACKS

BLE host, GATT, Wi-Fi, 6LoWPAN

Embedded software services

From first boot on FPGA to qualified production stacks — the same team, end to end.

BU

SoC & board bring-up

Bootloader, BSP, first boot on FPGA

OS

RTOS & Linux

FreeRTOS, Zephyr, Yocto Linux

DR

Device drivers

PCIe, Ethernet, USB, SD/MMC

WL

Wireless stacks

BLE 5 host, GATT, Wi-Fi, 6LoWPAN

MC

Motor control & ML

BLDC vector control, on-MCU ML

CI

FW validation & CI

Automated FW regression, Jenkins

Case study: RISC-V Core-IP software stack

Keeping bare-metal software in lock-step with a continuously evolving CPU IP.

CHALLENGE

200+ core configurations — single core to 16-core multi-cluster — each needing a correct BSP and validated software on every RTL drop.

RAITON EXECUTION

Owned the BSP generator and validation suite with CI/CD; root-caused failures across VCS simulation and Xilinx FPGA, working daily with RTL, DV and PD teams.

CUSTOMER IMPACT

Every configuration shipped with validated software; faster field customisation and tighter silicon–software alignment at release.

Case study: wireless IoT MCU platform

Qualified connectivity stacks that ship with the silicon — not months after it.

SCOPE

Bluetooth 5.0 LE host stack and GATT profiles, Wi-Fi host driver on Linux and RTOS, and an IoT gateway reference platform with cloud connectivity.

EXECUTION

Designed, ported and qualified the stacks across Windows, Linux and FreeRTOS; customised profiles (A2DP, HFP, MAP) per customer; built open-source starter kits.

WHY IT MATTERS

Customers evaluated and designed-in the MCU faster, with production-ready software reducing their own integration effort.

Case study: motor control & edge ML

Proving a microcontroller’s silicon features with application firmware that customers can ship.

CHALLENGE

A vector-engine MCU family needed BLDC motor-control firmware for a leading power-tool maker, plus on-device ML and IIoT 4.0 (TSN) demonstrators.

RAITON EXECUTION

Stood up a motor-control team from scratch; delivered the single-design firmware, ported and optimised ML algorithms to the MCU, and built the TSN proof of concept.

CUSTOMER IMPACT

Silicon differentiators became demonstrable in weeks — giving sales a working reference and customers a validated starting point.

Flexible engagement models

Scale expertise to match programme phase, urgency and ownership.

01 **Managed work package**

Outcome-led scope with Raiton ownership

02 **Embedded pod**

A ready team inside your programme

03 **Specialist augmentation**

Targeted senior capability where needed

04 **Build–operate–transfer**

Stand up capability, then transition

Why Raiton

A semiconductor execution partner — not a staffing vendor.

01

Silicon-first thinking

02

Senior hands-on talent

03

End-to-end accountability

04

Domain-specific depth

05

Evidence-led execution

06

Flexible, India-based scale

Let’s build your silicon together.

Our vision: become the long-term silicon execution partner for AI-native semiconductor companies.

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